



PATENT APPLICATION

THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of

Docket No: Q60074

Sang-ug KANG, et al.

Appln. No.: 09/771,632

Group Art Unit: 2631

Confirmation No.: 1274

Examiner: PHILIPPE, GIMS S.

Filed: January 30, 2001

For: VIDEO CODEC SYSTEM, METHOD FOR PROCESSING DATA BETWEEN SYSTEM
AND HOST SYSTEM, AND ENCODING/DECODING CONTROL METHOD IN THE
SYSTEM

SUBMISSION OF APPEAL BRIEF

MAIL STOP APPEAL BRIEF - PATENTS

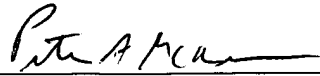
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith please find an Appeal Brief. A check for the statutory fee of \$500.00 is attached. The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account. A duplicate copy of this paper is attached.

Respectfully submitted,

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Date: June 12, 2006



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APPEAL BRIEF UNDER 37 C.F.R. § 41.37

MAIL STOP APPEAL BRIEF - PATENTS

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

In accordance with the provisions of 37 C.F.R. § 41.37, Appellant submits the following:

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I. REAL PARTY IN INTEREST

Based on the information supplied by the Appellant, and the best of Appellant's legal representative's knowledge, the real party in the interest is the assignee, SAMSUNG ELECTRONICS CO., LTD. The Assignment was recorded on January 30, 2001, at Reel 011507, Frame 0446.

II. RELATED APPEALS AND INTERFERENCES

To the best knowledge and belief of Appellant, the Assignee and the undersigned attorney, there are no other appeals or interferences before the Board of Appeals and Interferences (“the Board”) that will directly affect or be affected by the Board’s decision in the present Appeal.

III. STATUS OF CLAIMS

Claim 6 is pending in the application.

Claims 1-5 have been withdrawn from consideration pursuant to an Election of Species Requirement dated November 26, 2004.

Claim 6 stands finally rejected under 35 U.S.C. § 102(b) as being anticipated by Woo et al. (USP 5,7812,788).

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IV. STATUS OF AMENDMENTS

No Amendments have been filed in this application.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

The present invention relates to an encoding/decoding control method in a video codec system which is implemented in a processor independent from a host system (see claim 6). An embodiment of the invention is described in the specification with reference to Fig. 4.

Referring to FIG. 4, with the start command, the ICM 110 configures the TSR 120 so that the encoder 140 and/or decoder 160 can be performed. That is, `tsr[10]` and/or `tsr[11]` are reset in step 400. Then, the encoder 140 and/or decoder 160 checks the corresponding bit, that is, `tsr[10]` and `tsr[11]`, respectively, to determine whether or not to perform encoding and/or decoding in step 410.

The encoder buffer 150 and decoder buffer 170 show their statuses in the corresponding bits of the TSR 120, that is, in one of `tsr[0]~tsr[3]` and one of `tsr[4]~tsr[7]`, respectively in step 420. Then, the ICM 110 controls the encoder 140 and decoder 160 through the CIR 130 based on the statuses of the encoder buffer 150 and decoder buffer 170 written in the TSR 120 in step 430.

For example, as for the encoder buffer 150, when `tsr[0]=1`, the ICM 110 raises the priority level of the encoder 140. When `tsr[1]=1`, the ICM 110 stops the operation of the encoder 140, and sets `tsr[10]` to '1', and `tsr[14]` to '1'. When `tsr[2]=1`, and when a predetermined time has not passed when `tsr[0]=1`, the ICM 110 lowers the priority level of the encoder 140. When a predetermined time has not passed when `tsr[1]=1`, the ICM 110 raises the priority level of the

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encoder 140. To control more precisely, $\text{tsr}[3]=1$ and $\text{tsr}[7]=1$ are determined by the designer, and handled in the same way as $\text{tsr}[2]=1$ and $\text{tsr}[6]=1$.

As for the decoder buffer 170, when $\text{tsr}[4]=1$, the ICM 110 stops the operation of the decoder 160 and sets $\text{tsr}[11]$ to '1'. When $\text{tsr}[5]=1$, the decoder buffer 170 cannot be used and $\text{tsr}[13]$ is set to '1'. When $\text{tsr}[6]=1$, and when a predetermined time has not passed when $\text{tsr}[4]=1$, the ICM 110 raises the priority level of the decoder 160. When a predetermined time has not passed when $\text{tsr}[5]=1$, the ICM 110 lowers the priority level of the decoder 160.

As a result, referring to the status of each buffer, the ICM 110 controls operations such as stop and start operations of the encoder 140 and decoder 160 so that each buffer is not in an empty or full status. See the specification, at page 14, line 14 to page 15, line 21.

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VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The sole issue to be determined on appeal is whether claim 6 is properly rejected under 35 U.S.C. §102(b) as being anticipated by United States patent NO. 5,781,788 to Woo et al.

VII. ARGUMENT

Appellant submits that claim 6 is not anticipated by Woo et al because Woo et al fails to disclose each and every feature of the claim.

In a Response submitted July 22, 2005 to the Office Action dated April 22, 2005, Appellant submitted that Woo et al does not disclose “(b) determining whether or not to perform encoding and/or decoding, by checking a reset of the task status register in the encoder and/or decoder”, as required by claim 6, and several arguments were presented supporting this (see pages 2 and 3 of Appellant’s Response of July 22, 2005). In the Office Action dated October 10, 2005, the Examiner responded to each of these arguments. Appellant respectfully disagrees, however, with the Examiner’s response to these arguments.

First, Appellant argued in the July 22, 2005 Response that Woo does not teach in any way determining whether or not to perform encoding and/or decoding by checking a reset of the task status register (page 2, 4th paragraph). The Examiner responded by stating that the reset step of Fig. 5 of Woo is performed in a buffer, which is the claimed “register” (Office Action of October 12, 2005, paragraph bridging pages 2 and 3; see also Advisory Action of February 17, 2006, page 2). Appellant submits, however, that there is no teaching that the step 202 of Fig. 5 is performed in a buffer. Woo merely teaches that Fig. 5 illustrates the steps of a method 200 for rate buffer control (col. 13, lines 48-49), and does not teach that step 202 is performed in a buffer. The Examiner also states that Woo discloses, at col. 5, lines 24-34, encoding “by performing interrogation of the register file. Such interrogation as suggested by Woo is the status checking as claimed by the applicant. In addition, the steps taken to monitor the behavior

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of the coding/decoding process is understood as being the step where a decision has to be made in order to determine whether coding/decoding is necessary. Further, in col. 7, lines 15-20, Woo discloses a step of specifying the status information by register.” (Office Action of October 12, 2005, paragraph bridging pages 2 and 3; see also Advisory Action of February 17, 2006, page 2). Appellant respectfully disagrees with each of these statements.

Regarding the Examiner’s statement, that Woo discloses, at col. 5, lines 24-34, encoding “by performing interrogation of the register file”, there is no disclosure by Woo of encoding by performing interrogation of the register file. Woo merely teaches that the user can use the register file 40 to control, adjust and monitor operations of the video codec. There is no teaching that the reset of step 202 of Fig. 5 has any relation to this register file. The Examiner states: “Such interrogation as suggested by Woo is the status checking as claimed by the applicant.” But the Examiner has not demonstrated that the reset step 202 of Woo is related to the register file 40. In an anticipation rejection, there must be more than a suggestion. For an anticipation rejection, a single reference must teach every element of the claim expressly, implicitly or inherently. The Examiner has not shown that the step 20 of Fig. 5 of Woo is related to the file register 40. The Examiner’s allegation that this is suggested is not enough to support an anticipation rejection.

Also, in the Response submitted July 22, 2005 to the Office Action dated April 22, 2005, it was argued that there is no teaching or suggestion in Woo of “(c) making pre-assigned bits of the task status register indicate buffer statuses of an encoder buffer and a decoder buffer” (page 3 of the Response). In the Office Action of October 12, 2005, the Examiner refers to Woo at col.

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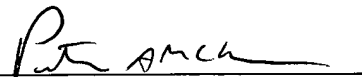
13, lines 50-51 as disclosing the “pre-assigned number of bits” (page 3, 2nd full paragraph). Appellant submits, however, that disclosing a “pre-assigned number of bits” does not meet the language of the claim. That is, claim 6 recites “making pre-assigned bits of the task status register indicate buffer statuses of an encoder buffer and a decoder buffer.” The portion of the reference cited by the Examiner discloses loading a target number of bits per frame, but does not disclose anything with regard to pre-assigned bits of a register. A pre-assigned number of bits is not related to pre-assigned bits.

Appellant submits that claim 6 is not anticipated by Woo et al at least for the reasons presented above and requests the Board not to sustain the rejection of claim 6.

Unless a check is submitted herewith for the fee required under 37 C.F.R. §41.37(a) and 1.17(c), please charge said fee to Deposit Account No. 19-4880.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,


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CLAIMS APPENDIX

CLAIM 6 ON APPEAL:

6. An encoding/decoding control method in a video codec system which is implemented in a processor independent from a host system, the encoding/decoding control method comprising the steps of:

(a) resetting pre-assigned bits of a task status register in the video codec system so that an encoder and/or decoder can operate when a start command is input from the host system;

(b) determining whether or not to perform encoding and/or decoding, by checking a reset of the task status register in the encoder and/or decoder;

(c) making pre-assigned bits of the task status register indicate buffer statuses of an encoder buffer and a decoder buffer; and

(d) checking the buffer statuses of the encoder buffer and the decoder buffer written in the task status register, and then controlling tasks of the encoder and the decoder.

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EVIDENCE APPENDIX:

NONE

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RELATED PROCEEDINGS APPENDIX

NONE